Scripting GPUs with PyOpenCL

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Thanks

- Tim Warburton (Rice)
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- David Garcia
- Nicolas Pinto (MIT)
- PyOpenCL, PyCUDA contributors
- Nvidia Corporation

- 1 Intro: GPUs, OpenCL
- 2 GPU Programming with PyOpenCL
- 3 Additional Topics
- 4 Playtime!
- 5 Conclusions





- 1 Intro: GPUs, OpenCL
 - What and Why?
 - Bird's eye view of OpenCL
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GPU Computing?

- Design target for CPUs:
 - Make a single thread very fast
 - Hide latency through large caches
 - Predict, speculate







GPU Computing?

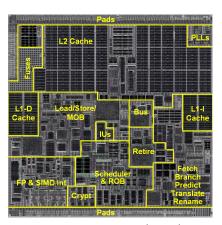
- Design target for CPUs:
 - Make a single thread very fast
 - Hide latency through large caches
 - Predict, speculate
- GPU Computing takes a different approach:
 - Throughput matters single threads do not
 - Hide latency through parallelism
 - Let programmer deal with "raw" storage hierarchy



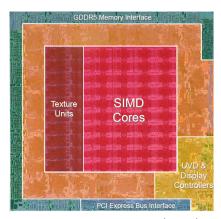




GPU-CPU Bird's Eye Comparison



Floorplan: VIA Isaiah (2008) 65 nm, 4 SP ops at a time, 1 MiB L2.



Floorplan: AMD RV770 (2008)
55 nm, 800 SP ops
at a time.

GPU Architecture (e.g. Nvidia GT200)



- 1 GPU = 30 SIMD cores
- 1 SIMD core: 32 × 32 PCs, HW Sched + 1 ID (1/4 clock) + 8 SP + 1 DP + 16 KiB Shared + 32 KiB Reg
- Device ↔ RAM: **140 GB/s**
- Device ↔ Host: 6 GB/s
- User manages memory hierarchy





GPU Programming: Gains and Losses

| Gains | Losses |
|---|--------|
| Memory Bandwidth (140 GB/s vs. 12 GB/s) Compute Bandwidth (Peak: 1 TF/s vs. 50 GF/s, Real: 200 GF/s vs. 10 GF/s) ○ Data-parallel programming | |
| | |



GPU Programming: Gains and Losses

Gains

- ◆ Memory Bandwidth (140 GB/s vs. 12 GB/s)
- Compute Bandwidth (Peak: 1 TF/s vs. 50 GF/s,

Real: 200 GF/s vs. 10 GF/s)

Data-parallel programming

Losses

- Tuning hardware-specific
- Data size

 Alg. design
- Cheap branches (i.e. ifs)
- Fine-grained malloc *)
- Recursion *)
- Function pointers *)

*) Possibly less problematic soon.





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What is OpenCL?

OpenCL (Open Computing Language) is an open, royalty-free standard for general purpose parallel programming across CPUs, GPUs and other processors. [OpenCL 1.1 spec]

- Vendor-neutral, unlike Nvidia CUDA
 - though rather similar to it

Defines:

- Host-side programming interface (library)
- Device-side programming language (!)

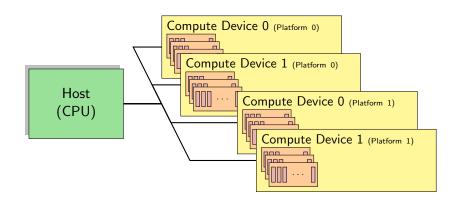




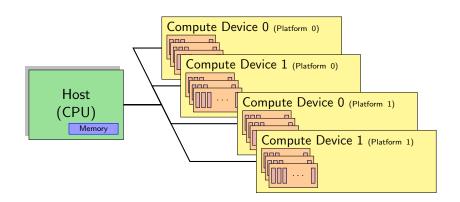


Host (CPU)

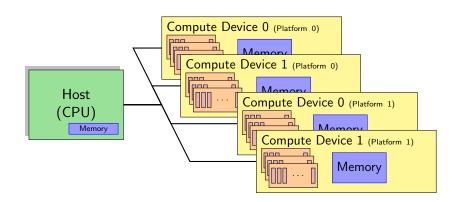




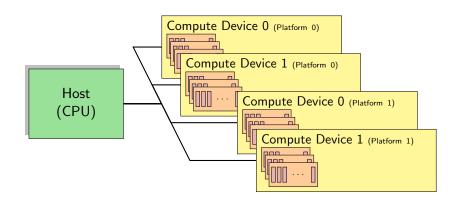




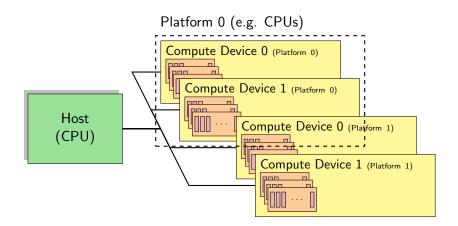




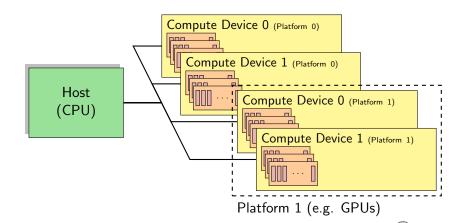




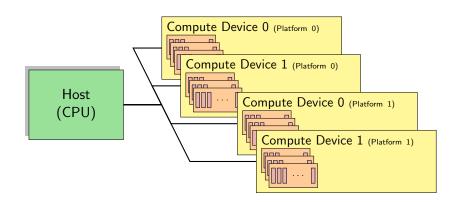




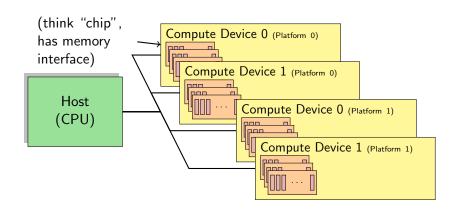




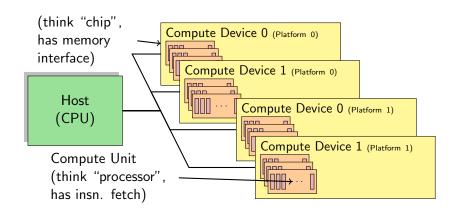
BROWN



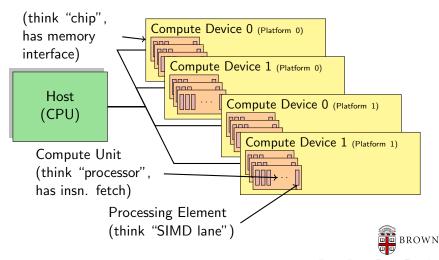


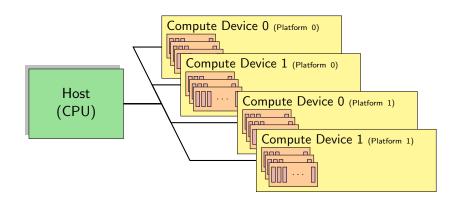




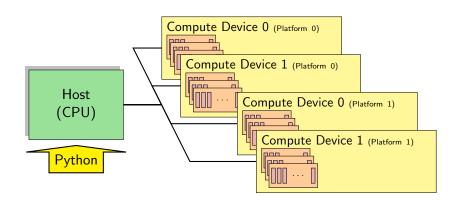




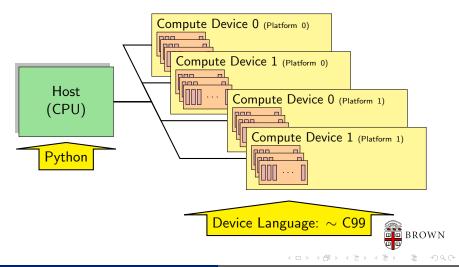




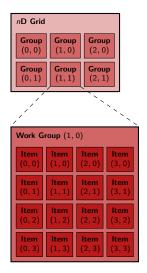








OpenCL: Execution Model

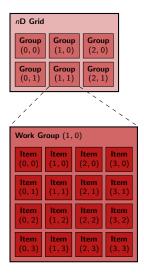


- Two-tiered Parallelism
 - Grid = $N_x \times N_y \times N_z$ work groups
 - Work group = $S_x \times S_y \times S_z$ work items
 - Total: $\prod_{i \in \{x,y,z\}} S_i N_i$ work items





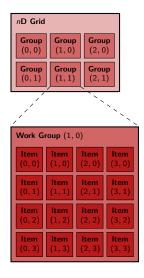
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 - Total: $\prod_{i \in \{x,y,z\}} S_i N_i$ work items
- Comm/Sync only within work group
 - Work group maps to compute unit
- Grid/Group \approx outer loops in an algorithm
- Device Language:
 get_{global,group,local}_{id,size}
 (axis)



Why do Scripting for OpenCL?

- Compute Devices are everything that scripting languages are not.
 - Highly parallel
 - Very architecture-sensitive
 - Built for maximum FP/memory throughput
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 - Scripting fast enough







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- CPU: largely restricted to control tasks ($\sim 1000/\text{sec}$)
 - Scripting fast enough
- Python + OpenCL = PyOpenCL







Questions?

?



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```
import pyopencl as cl, numpy
 3
    a = numpy.random.rand(256**3).astype(numpy.float32)
 4
 5
    ctx = cl. create\_some\_context()
 6
    queue = cl.CommandQueue(ctx)
 8
    a_dev = cl. Buffer(ctx, cl.mem_flags.READ_WRITE, size=a.nbytes)
    cl. engueue_write_buffer (queue, a_dev, a)
10
11
    prg = cl. Program(ctx, """
12
         __kernel void twice( __global float *a)
        \{ a[get\_global\_id (0)] *= 2; \}
13
14
        """ ). build ()
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    prg.twice(queue, a.shape, (1,), a_dev)
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Dive into PyOpenCL: Getting Results

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    prg.twice(queue, a.shape, (1,), a_dev)
17
18
     result = numpy.empty_like(a)
    cl . enqueue_read_buffer (queue, a_dev, result ). wait()
19
    import numpy.linalg as la
20
21
     assert la.norm(result -2*a) == 0
```

Dive into PyOpenCL: Grouping

```
8
    a_dev = cl. Buffer(ctx, cl.mem_flags.READ_WRITE, size=a.nbytes)
    cl . enqueue_write_buffer (queue, a_dev, a)
10
11
    prg = cl. Program(ctx, """
12
         __kernel void twice( __global float *a)
        { a[get_local_id (0)+ get_local_size (0)*get_group_id (0)] *= 2; }
13
        """). build()
14
15
16
    prg.twice(queue, a.shape, (256,), a_dev)
17
18
     result = numpy.empty_like(a)
    cl . enqueue_read_buffer (queue, a_dev, result ). wait()
19
    import numpy.linalg as la
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21
     assert la.norm(result -2*a) == 0
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Log into your assigned machine:

- 1 ssh NAME@haamster.rice.edu
- 2 ssh teramite or ssh slate

In your home directory, find "1-intro/intro.py".

Try running it (on the right GPU).

http://tiker.net/tmp/scipy10-pyopencl-tut.tar.gz

Thinking about GPU programming

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$$1$$
 ... compute $c_i = a_i b_i$?

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- 1 ... compute $c_i = a_i b_i$?
- 2 ... use groups of 16×16 work items?

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Thinking about GPU programming

- 1 ... compute $c_i = a_i b_i$?
- 2 ... use groups of 16×16 work items?
- 3 ... benchmark 1 work item per group against 256 work items per group? (Use time.time() and .wait().)

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Contexts

 $\begin{array}{lll} {\sf context} &= {\sf cl}.\,{\sf Context}({\sf devices} {=} {\sf None} \mid [{\sf dev1},\,{\sf dev2}],\,\,{\sf dev_type} {=} {\sf None}) \\ {\sf context} &= {\sf cl}.\,{\sf create_some_context}(\,\,{\sf interactive} = {\sf True}) \end{array}$



- Spans one or more Devices
- Create from device type or list of devices
 - See docs for cl.Platform, cl.Device
- dev_type: *DEFAULT*, ALL, CPU, GPU
- Needed to...
 - ...allocate Memory Objects
 - ... create and build Programs
 - ...host Command Queues
 - ...execute Grids





Command Queues and Events

```
queue = cl. CommandQueue(context, device=None,
  properties = None | [(prop, value ),...])
```

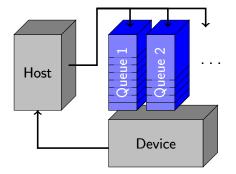
- Attached to single device
- event = enqueue_XXX(queue, ..., wait_for=[evt1. evt2])
- event.wait()
- Command in queue implicitly waits for previous command's completion





OpenCL: Command Queues

- Host and Device run asynchronously
- Host submits to queue:
 - Computations
 - Memory Transfers
 - Sync primitives
 -
- Host can wait for drained queue
- Multiple Queues:Can overlapCompute + Transfer







```
✓ OK
```

```
\label{eq:alpha} $$a = \underset{\mbox{\sc numpy.random.rand}}{\text{\sc numpy.random.rand}} (256**3).$$ a_dev = ${\tt cl.Buffer}(ctx, \ \c l.mem_flags.READ_WRITE, size=a.nbytes)$$ ${\tt cl.enqueue\_write\_buffer}(queue, a_dev, a)$
```

✓ OK

```
\label{eq:alpha} \begin{split} & = \underset{\mbox{\sc numpy.random.rand}}{\text{\sc numpy.random.rand}} (256**3).\mbox{\sc stype}(\mbox{\sc numpy.float32}) \\ & = _{\mbox{\sc cl.}} \mbox{\sc Buffer}(\mbox{\sc ct.} \mbox{\sc mem\_flags.READ\_WRITE}, \mbox{\sc size} = a.nbytes) \\ & = _{\mbox{\sc cl.}} \mbox{\sc cl.} \mbox{\sc enqueue\_write\_buffer} (\mbox{\sc queue}, \ a\_dev, \ a) \end{split}
```

* Crash

✓ OK

```
\label{eq:alpha_state} \begin{split} & = \underset{\mbox{numpy.random.rand}}{\text{numpy.random.rand}} (256**3).\text{astype}(\underset{\mbox{numpy.float32}}{\text{numpy.float32}}) \\ & = \underset{\mbox{cl. enqueue\_write\_buffer}}{\text{cl. enqueue\_write\_buffer}} (\underset{\mbox{queue, a\_dev, a}}{\text{cl. enqueue\_write\_buffer}} (\underset{\mbox{queue, a\_dev, a}}{\text{cl. enqueue\_write\_buffer}}) \end{split}
```

* Crash

```
\label{eq:a_dev} $$ a_dev = \mbox{cl. Buffer(ctx, cl. mem_flags.READ_WRITE, size=256**3*4)} $$ cl. enqueue_write_buffer (queue, a_dev, numpy.random.rand(256**3).astype(numpy.float32)) $$
```

✓ OK

```
\label{eq:a_dev} $$a\_dev = \mbox{cl. Buffer(ctx, cl.mem_flags.READ_WRITE, size=256**3*4)}$$ cl. enqueue_write_buffer (queue, a_dev, numpy.random.rand(256**3).astype(numpy.float32), is_blocking = True)
```

✓ OK (usually!)

```
\label{eq:alpha} \begin{split} & = \underset{\mbox{numpy.random.rand}}{\text{numpy.random.rand}} (256**3). \\ & \text{a\_dev} = \underset{\mbox{cl.}}{\text{cl.}} \text{Buffer}(\text{ctx}, \underset{\mbox{cl.}}{\text{cl.}} \text{mem\_flags.READ\_WRITE}, \ \text{size} = \text{a.nbytes}) \\ & \text{cl.} \ \text{enqueue\_write\_buffer} \left( \text{queue}, \ \text{a\_dev}, \ \text{a} \right) \end{split}
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```

buf = cl. Buffer(context, flags, size=0, hostbuf=None)

- Chunk of device memory
- No type information: "Bag of bytes"
- Specify hostbuf or size (or both)
- hostbuf: Needs Python Buffer Interface e.g. numpy.ndarray, str.
- flags:
 - READ_ONLY/WRITE_ONLY/READ_WRITE
 - {ALLOC, COPY, USE}_HOST_PTR





Memory Objects: Buffers

buf = cl. Buffer(context, flags, size = 0, hostbuf = None)

- Passed to device code as pointers
 (e.g. float *, int *)
- enqueue_{read,write}_buffer(
 queue, buf, hostbuf)
- Can be mapped into host address space: cl.MemoryMap.







prg = cl. Program(context, src)

- src: OpenCL device code
 - Derivative of C99
 - Functions with __kernel attribute can be invoked from host
- kernel = prg.kernel_name
- * kernel(queue, (G_x, G_y, G_z) , (S_x, S_y, S_z) , arg, ..., wait_for=None)

(Note: local_size used to be keyword argument.)





Program Objects

$$kernel \, \big(\mathsf{queue}, \, \, \big(\mathsf{Gx}, \mathsf{Gy}, \mathsf{Gz} \big), \, \, \big(\mathsf{Sx}, \mathsf{Sy}, \mathsf{Sz} \big), \, \, \mathsf{arg} \, , \, \, \, \ldots, \, \, \, \, \mathsf{wait_for} \, = \, \mathsf{None} \big)$$



arg may be:

- None (a NULL pointer)
- numpy sized scalars: numpy.int64,numpy.float32,...
- Anything with buffer interface: numpy.ndarray, str
- Buffer Objects
- Also: cl.Image, cl.Sampler, cl.LocalMemory





obrain objects

 $kernel \, \big(\mathsf{queue}, \, \, \big(\mathsf{Gx}, \mathsf{Gy}, \mathsf{Gz} \big), \, \, \big(\mathsf{Sx}, \mathsf{Sy}, \mathsf{Sz} \big), \, \, \mathsf{arg} \,, \, \, \, \ldots, \, \, \, \, \mathsf{wait_for} \, = \, \mathsf{None} \big)$

Explicitly sized scalars:

***** Annoying, error-prone.



Better:

kernel.set_scalar_arg_dtypes([
 numpy.int32, None,
 numpy.float32])

Use None for non-scalars.





Single-Instruction Multiple-Data in OpenCL

OpenCL exposes two different forms of SIMD computing:

- Explicit: Use (e.g.) float2, ..., float16.
- Implicit: Adjacent work items get mapped to SIMD lanes (implemented in hardware or software)



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 \rightarrow "Work Item" \neq "Thread"!

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do_the_rest():

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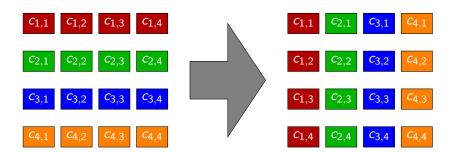
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Example: Matrix Transpose





Transpose? Simple Enough!

```
self . kernel = cl. Program(ctx,
kernel
void transpose(
  __global float *a_t, __global float *a,
  unsigned a_width, unsigned a_height)
  int read_idx = get_global_id(0) + get_global_id(1) * a_width;
  int write_idx = get_global_id (1) + get_global_id (0) * a_height;
  a_t [ write_idx ] = a[read_idx ];
"""). build (). transpose
```

Measuring Performance

Writing high-performance Codes

Mindset: What is going to be the limiting factor?

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Evaluate

- Know your peak throughputs (roughly)
- Are you getting close?
- Are you tracking the right limiting factor?

Intro PyOpenCL Additional Topics Playtime! Conclusions First Contact Details Memory Synchronization PyOpenCL

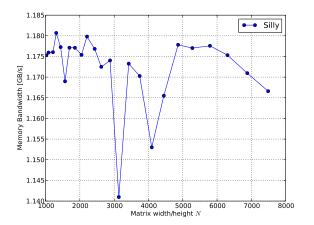
Performance: Matrix transpose

Very likely: Bound by memory bandwidth.



Performance: Matrix transpose

Very likely: Bound by memory bandwidth.



Fantastic! Far slower than CPU. Why?

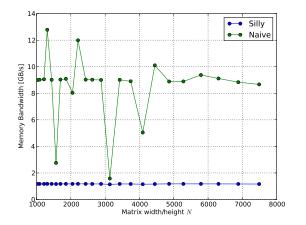


Intra-device Work Distribution

Again: Work Groups

- Work group size matters. A lot.
- Determines work distribution among processors
- Optimal size? Up to experimentation

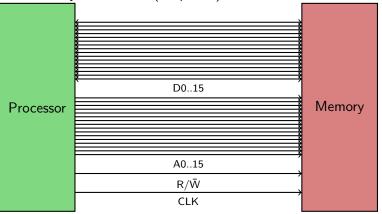
Performance: Matrix transpose



Better. $1.5 \times$ faster than CPU-not great. Why?

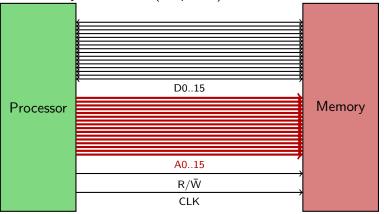




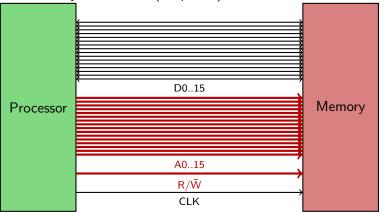






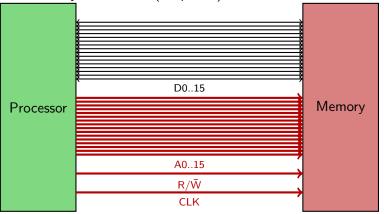




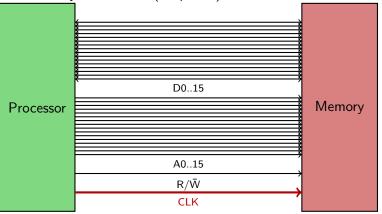




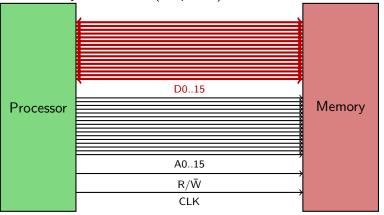










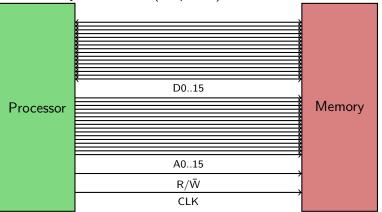




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Aside: How does computer memory work?

One memory transaction (simplified):



Observation: Access (and addressing) happens in bus-width-size "chunks".



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Memory for Parallel Machines

Problem

Memory chips have only one data bus.

So how can multiple threads read multiple data items from memory simultaneously?

Memory for Parallel Machines

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Memory chips have only one data bus.

So how can multiple threads read multiple data items from memory simultaneously?

Solutions: Parallel Access to Memory

- Split a really wide data bus, but have only one address bus
- Have many "small memories" ("banks") with separate data and address busses, select by address LSB.

```
self . kernel = cl . Program(ctx,
__kernel
void transpose(
  __global float *a_t, __global float *a,
  unsigned a_width, unsigned a_height)
  int read_idx = get_global_id (0) + get_global_id (1) * a_width;
  int write_idx = get_global_id (1) + get_global_id (0) * a_height;
  a_t[write_idx] = a[read_idx];
"""). build (). transpose
```

```
self . kernel = cl . Program(ctx,
__kernel
void transpose(
  __global float *a_t, __global float *a,
  unsigned a_width, unsigned a_height)
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  int write_idx = get_global_id (1) + get_global_id (0) * a_height;
  a_t[write_idx] = a[read_idx];
"""). build (). transpose
```

Reading from global mem:



stride: 1

```
self . kernel = cl . Program(ctx,
__kernel
void transpose(
  __global float *a_t, __global float *a,
  unsigned a_width, unsigned a_height)
  int read_idx = get_global_id (0) + get_global_id (1) * a_width;
  int write_idx = get_global_id (1) + get_global_id (0) * a_height;
  a_t[write_idx] = a[read_idx];
"""). build (). transpose
```

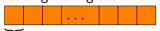
Reading from global mem:



stride: $1 \rightarrow$ one mem.trans.

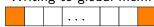
```
self . kernel = cl . Program(ctx,
__kernel
void transpose(
  __global float *a_t, __global float *a,
  unsigned a_width, unsigned a_height)
  int read_idx = get_global_id (0) + get_global_id (1) * a_width;
  int write_idx = get_global_id (1) + get_global_id (0) * a_height;
  a_t[write_idx] = a[read_idx];
"""). build (). transpose
```

Reading from global mem:



stride: $1 \rightarrow$ one mem.trans.

Writing to global mem:



stride: 16

```
self . kernel = cl . Program(ctx,
__kernel
void transpose(
  __global float *a_t, __global float *a,
  unsigned a_width, unsigned a_height)
  int read_idx = get_global_id (0) + get_global_id (1) * a_width;
  int write_idx = get_global_id (1) + get_global_id (0) * a_height;
  a_t[write_idx] = a[read_idx];
"""). build (). transpose
```

Reading from global mem:

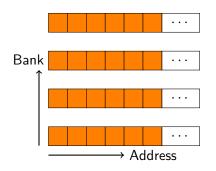


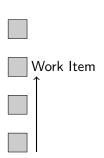
stride: $1 \rightarrow$ one mem.trans.

Writing to global mem:

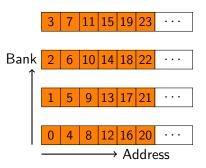


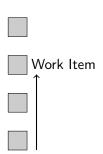
stride: $16 \rightarrow 16$ mem.trans.!



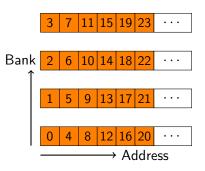


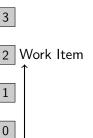




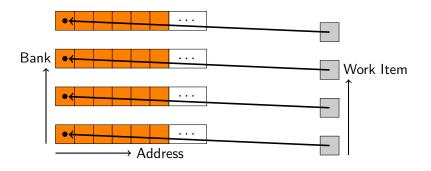






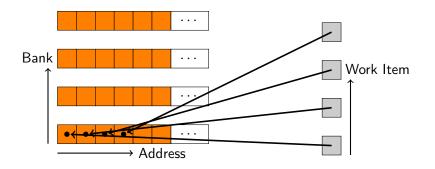






OK: local_variable[get_local_id(0)], (Single cycle)





Bad: local_variable[BANK_COUNT*get_local_id(0)]
(BANK_COUNT cycles)



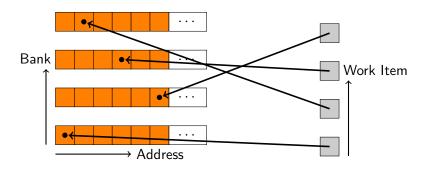


OK: local_variable[(BANK_COUNT+1)*get_local_id(0)] (Single cycle)



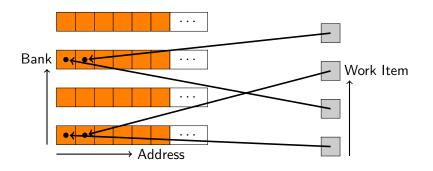
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Local Memory: Banking



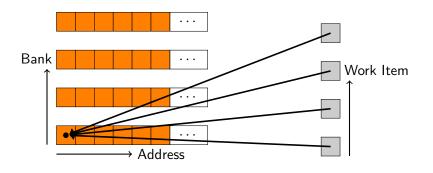
OK: local_variable[ODD_NUMBER*get_local_id(0)] (Single cycle)





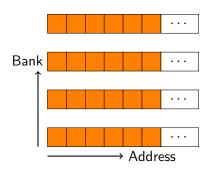
Bad: local_variable[2*get_local_id(0)]
(BANK_COUNT/2 cycles)

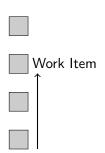




OK: local_variable[f(blockIdx)]
(Broadcast-single cycle)







Nvidia hardware has 16 banks. Work item access local memory in groups of 16.





Transpose: Idea

- Global memory dislikes non-unit strides.
- Local memory doesn't mind.



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Idea

- Don't transpose element-by-element.
- Transpose block-by-block instead.





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Transpose: Idea

- Global memory dislikes non-unit strides.
- Local memory doesn't mind.

Idea

- Don't transpose element-by-element.
- Transpose block-by-block instead.
- Read untransposed block from global and write to local
- 2 Read block transposed from local and write to global



Illustration: Blockwise Transpose

| $C_{1,1}$ | C _{1,2} | C _{1,3} | C _{1,4} | $C_{1,1}^T$ | $C_{2,1}^T$ | $C_{3,1}^T$ | $C_{4,1}^T$ |
|------------------|------------------|------------------|------------------|-------------------------|-------------|-------------|-------------|
| C _{2,1} | C _{2,2} | C _{2,3} | C _{2,4} | $C_{1,2}^{\mathcal{T}}$ | $C_{2,2}^T$ | $C_{3,2}^T$ | $C_{4,2}^T$ |
| C _{3,1} | C _{3,2} | C _{3,3} | C _{3,4} | $C_{1,3}^T$ | $C_{2,3}^T$ | $C_{3,3}^T$ | $C_{4,3}^T$ |
| C _{4,1} | C _{4,2} | C _{4,3} | C _{4,4} | $C_{1,4}^T$ | $C_{2,4}^T$ | $C_{3,4}^T$ | $C_{4,4}^T$ |



Part 1/3:

```
#define BLOCK_SIZE 16
#define A_BLOCK_STRIDE (BLOCK_SIZE * a_width)
#define A_T_BLOCK_STRIDE (BLOCK_SIZE * a_height)

__kernel void transpose(
__global float *a_t, __global float *a,
unsigned a_width, unsigned a_height)
```

Part 2/3:

```
__local float a_local [BLOCK_SIZE][BLOCK_SIZE];
int base_idx_a
  get_group_id(0) * BLOCK_SIZE +
  get_group_id(1) * A_BLOCK_STRIDE;
int base_idx_a_t =
  get_group_id(1) * BLOCK_SIZE +
  get_group_id(0) * A_T_BLOCK_STRIDE;
int glob_idx_a
  base_idx_a + get_local_id(0)
  + a_width * get_local_id (1);
int glob_idx_a_t =
  base_idx_a_t + get_local_id(0)
 + a_height * get_local_id (1);
```

Part 3/3:

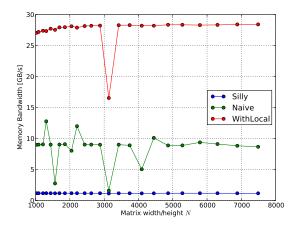
```
a_local [ get_local_id (1)][ get_local_id (0)] = a[glob_idx_a ];
barrier (CLK_LOCAL_MEM_FENCE);
a_t [ glob_idx_a_t ] = a_local [ get_local_id (0)][ get_local_id (1)];
}
```

Launch Code:

```
w, h = shape
return self . kernel (queue, (w, h), (16, 16),
     tgt, src, numpy.uint32(w), numpy.uint32(h))
```

Transpose example is 2-transpose/transpose.py in your home directory. Spot any bank conflicts? Tinker away!

Performance: Matrix transpose



Much better. Not peak, but good enough.



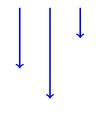


Outline

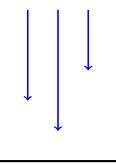
- 2 GPU Programming with PyOpenCL
 - First Contact
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 - Dealing with Space: Memory
 - Dealing with Time: Synchronization
 - What PyOpenCL brings to the Table



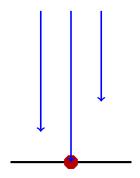




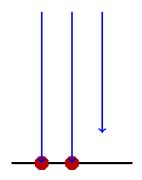




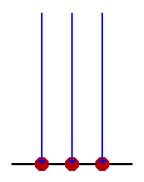




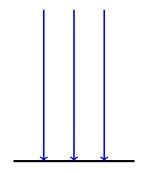




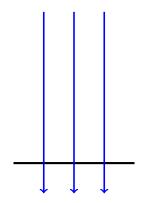














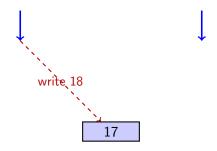
What is a Memory Fence?



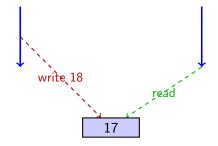


17

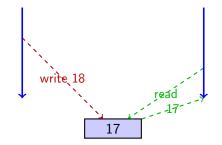




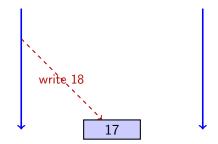




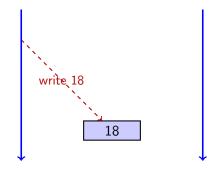




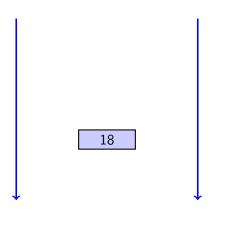


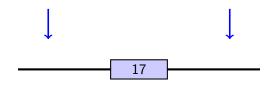




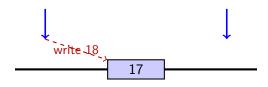




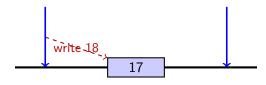




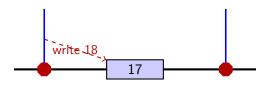




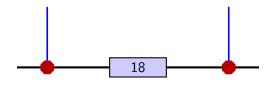




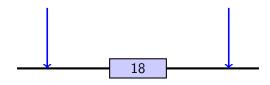




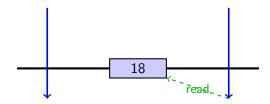




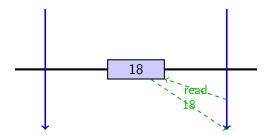














Recap: Concurrency and Synchronization

GPUs have layers of concurrency.

Each layer has its synchronization primitives.



Recap: Concurrency and Synchronization

GPUs have layers of concurrency.

Each layer has its synchronization primitives.

```
Intra-block:
barrier(...),
mem_fence(...)
... =
CLK_{LOCAL,GLOBAL}_MEM_FENCE
```

- Inter-block: Kernel launch
- CPU-GPU: Command queues, Events



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Synchronization between Groups

Golden Rule:

Results of the algorithm must be independent of the order in which work groups are executed.



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Synchronization between Groups

Golden Rule:

Results of the algorithm must be independent of the order in which work groups are executed.

Consequences:

- Work groups may read the same information from global memory.
- But: Two work groups may not validly write different things to the same global memory.
- Kernel launch serves as
 - Global barrier
 - Global memory fence





Outline

- 1 Intro: GPUs, OpenCL
- 2 GPU Programming with PyOpenCL
 - First Contact
 - A more Detailed Look
 - Dealing with Space: Memory
 - Dealing with Time: Synchronization
 - What PyOpenCL brings to the Table
- 3 Additional Topics
- 4 Playtime!
- 5 Conclusions





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PyOpenCL Philosophy



- Provide complete access
- Automatically manage resources
- Provide abstractions
- Allow interactive use
- Check for and report errors automatically
- Integrate tightly with numpy





PyOpenCL: Completeness



PyOpenCL exposes all of OpenCL.

For example:

- OpenCL 1.1
- Every GetInfo() query
- Images and Samplers
- Memory Maps
- Profiling and Synchronization
- GL Interop (example in source)





PyOpenCL: Completeness

PyOpenCL supports (nearly) every OS that has an OpenCL implementation.

- Linux
- OS X
- Windows







Automatic Cleanup

- Reachable objects (memory, streams, ...) are never destroyed.
- Once unreachable, released at an unspecified future time.
- Scarce resources (memory) can be explicitly freed. (obj.release())
- Correctly deals with multiple contexts and dependencies.







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PyOpenCL: Documentation







PyOpenCL: Vital Information

- http://mathema.tician.de/ software/pyopencl
- Complete documentation
- MIT License (no warranty, free for all use)
- Requires: numpy, Boost C++, Python 2.4+.
- Support via mailing list.







pyopencl.array: Simple Linear Algebra

pyopencl.array.Array:

- Meant to look and feel just like numpy.
 - p.a.to_device(ctx, queue, numpy_array)
 - $numpy_array = ary.get()$
- \blacksquare +, -, *, /, fill, sin, arange, exp, rand, ...
- Mixed types (int32 + float32 = float64)
- print cl_array for debugging.
- Allows access to raw bits
 - Use as kernel arguments, memory maps







Remember your first PyOpenCL program?

Abstraction is good:

```
import numpy
    import pyopencl as cl
    import pyopencl.array as cl_array
 4
 5
    ctx = cl. create\_some\_context()
    queue = cl.CommandQueue(ctx)
 8
    a_gpu = cl_array . to_device (
 9
             ctx, queue, numpy.random.randn(4,4).astype(numpy.float32))
    a_{doubled} = (2*a_{gpu}).get()
10
11
    print a_doubled
12
    print a_gpu
```



pyopencl.elementwise: Elementwise expressions

Avoiding extra store-fetch cycles for elementwise math:

```
n = 10000
a_gpu = cl_array . to_device (
        ctx, queue, numpy.random.randn(n).astype(numpy.float32))
b_gpu = cl_array . to_device (
        ctx, queue, numpy.random.randn(n).astype(numpy.float32))
from pyopencl.elementwise import ElementwiseKernel
lin\_comb = ElementwiseKernel(ctx,
        "float a, float *x, float b, float *y, float *z",
        "z[i] = a*x[i] + b*y[i]")
c_gpu = cl_array . empty_like(a_gpu)
lin_comb(5, a_gpu, 6, b_gpu, c_gpu)
import numpy.linalg as la
assert la.norm((c_gpu - (5*a_gpu+6*b_gpu)).get()) < 1e-5
```

Questions?



- 3 Additional Topics
 - Code Generation
 - Other GPU Gadgetry
 - GPU Architectures in more Detail.
 - Automatic GPU Programming





- 3 Additional Topics
 - Code Generation
 - Other GPU Gadgetry
 - GPU Architectures in more Detail
 - Automatic GPU Programming





The OpenCL Ecosystem: One Language, Many Devices

OpenCL generalizes over many types of devices:

- Multicore CPUs
- Various GPU architectures
- Accelerator boards





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Devices differ by

- Memory Types, Latencies, **Bandwidths**
- Vector Widths
- Units of Scheduling







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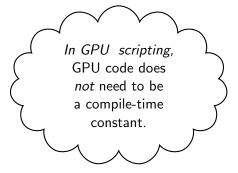
Optimally tuned code will (often) be different for each device



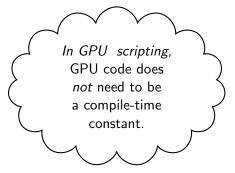


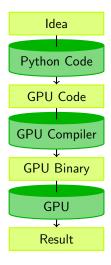


In GPU scripting,
GPU code does
not need to be
a compile-time
constant.

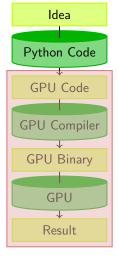


Idea



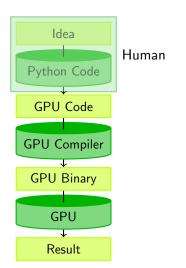




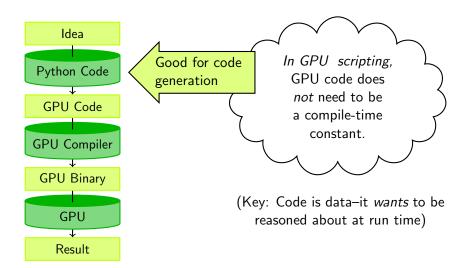


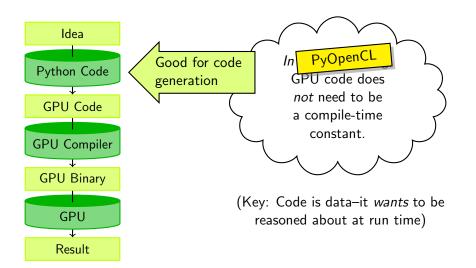
Machine











Machine-generated Code

Why machine-generate code?

- Automated Tuning (cf. ATLAS, FFTW)
- Data types
- Specialize code for given problem
- Constants faster than variables (→ register pressure)
- Loop Unrolling





PyOpenCL: Support for Metaprogramming

Three (main) ways of generating code:

- Simple %-operator substitution
- Use a templating engine (Jinja 2 works very well)
- codepy:
 - Build C syntax trees from Python
 - Generates readable, indented C

Many ways of evaluating code–most important one:

■ Exact device timing via events





RTCG via Templates

```
from jinja2 import Template
tpl = Template("""
    __kernel void twice( __global {{ type_name }} *tgt)
      int idx = get_local_id(0)
        + {{ local_size }} * {{ thread_strides }}
        * get_group_id (0);
      {% for i in range( thread_strides ) %}
          \{\% \text{ set offset } = i* \text{local\_size } \%\}
        tgt[idx + {{ offset }}] *= 2;
      {% endfor %}
rendered_tpl = tpl.render(type_name="float",
     local_size = local_size , thread_strides = thread_strides )
knl = cl. Program(ctx, str(rendered_tpl)). build(). twice
```

RTCG via AST Generation

```
from codepy.cgen import *
from codepy.cgen.opencl import \
        CLKernel, CLGlobal, CLRequiredWorkGroupSize
mod = Module([
    FunctionBody(
        CLKernel(CLRequiredWorkGroupSize((local_size,),
            FunctionDeclaration(Value("void", "twice"),
            arg_decls = [CLGlobal(Pointer(Const(POD(dtype, "tgt"))))]))),
        Block([
             Initializer (POD(numpy.int32, "idx"),
                " get_local_id(0) + %d * get_group_id(0)"
                % ( local_size * thread_strides ))
            1+[
            Statement("tgt[idx+%d] *= 2" % (o*local_size))
            for o in range( thread_strides )]
             ))])
knl = cl. Program(ctx, str(mod)).build(). twice
```

Outline

- 3 Additional Topics
 - Code Generation
 - Other GPU Gadgetry

 - Automatic GPU Programming





Collaborative (inter-block) Global Memory Update:





Collaborative (inter-block) Global Memory Update:





Collaborative (inter-block) Global Memory Update:





Collaborative (inter-block) Global Memory Update:



Atomic Global Memory Update:



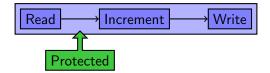




Collaborative (inter-block) Global Memory Update:



Atomic Global Memory Update:

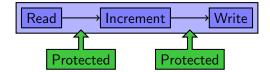




Collaborative (inter-block) Global Memory Update:



Atomic Global Memory Update:

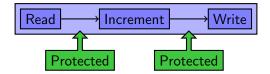




Collaborative (inter-block) Global Memory Update:



Atomic Global Memory Update:



How?

 $atomic_{-} \{add, inc, cmpxchg, \dots \} (int *global, int value);$





Even more GPU Gadgetry

Available in GPU code:

- Floating point intrinsics
 - native_sin(x), native_cos(x), etc.
 - Very fast
 - Less accurate, limited domains
- Vector types
 - \blacksquare int/float *n* for *n* in 1,2,3,4,8,...
 - Plus functions: load/store/sum/dot
 - Much saner than SSE intrinsics
- Images (r/w through texture units)
 - Can do filtering
 - Has some cache





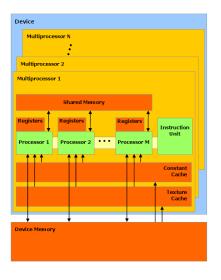


- 3 Additional Topics
 - Code Generation
 - Other GPU Gadgetry
 - GPU Architectures in more Detail
 - Automatic GPU Programming





GPU Architecture (e.g. Nvidia GT200)

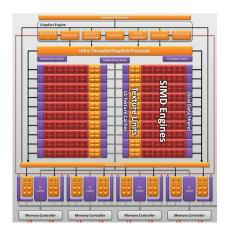


- 1 GPU = 30 SIMDs
- 1 SIMD = 1 ID (1/4 clock) + 8 SP + 1 DP + 16 KiB Shared + 32 KiB Reg + HW Sched
- Scalar cores, deep pipeline
- 32 scheduling slots
- DDR3 RAM (140 GB/s)
- PCle2 Host DMA (6 GB/s)
- Limited Caches





GPU Architecture (e.g. ATI RV870)



- 1 GPU = 20 SIMDs + 64 KiB Global Share + 4 × 128 KiB L2
- 1 SIMD = 1 ID + 16×5 SP + 16 DP + 32 KiB Share + HW Sched + 8 KiB L1
- GDDR5 RAM (150 GB/s)
- PCle2 Host DMA (6 GB/s)





- 3 Additional Topics
 - Code Generation
 - Other GPU Gadgetry
 - GPU Architectures in more Detail
 - Automatic GPU Programming





GPU programming can be time-consuming, unintuitive and error-prone.

- Obvious idea: Let the computer do it.
- One way: Smart compilers





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- Obvious idea: Let the computer do it.
- One way: Smart compilers
 - GPU programming requires complex tradeoffs
 - Tradeoffs require heuristics
 - Heuristics are fragile





GPU programming can be time-consuming, unintuitive and error-prone.

- Obvious idea: Let the computer do it.
- One way: Smart compilers
 - GPU programming requires complex tradeoffs
 - Tradeoffs require heuristics
 - Heuristics are fragile
- Another way: Dumb enumeration
 - Enumerate loop slicings
 - Enumerate prefetch options
 - Choose by running resulting code on actual hardware





Loo.py Example

Empirical GPU loop optimization:

```
a, b, c, i, j, k = [var(s) for s in "abcijk"]
n = 500
k = make_loop_kernel([
    LoopDimension("i", n),
    LoopDimension("j", n),
    LoopDimension("k", n),
    ], [
    (c[i+n*j], a[i+n*k]*b[k+n*j])
])

gen_kwargs = {
    "min_threads": 128,
    "min_blocks": 32,
    }
}
```

 \rightarrow Ideal case: Finds 160 GF/s kernel without human intervention.







Loo.py Status

Limited scope:

- Require input/output separation
- Kernels must be expressible using "loopy" model (i.e. indices decompose into "output" and "reduction")
- Enough for DG, LA, FD, ...







Loo.py Status

- Limited scope:
 - Require input/output separation
 - Kernels must be expressible using "loopy" model (i.e. indices decompose into "output" and "reduction")
 - Enough for DG, LA, FD, ...
- Kernel compilation limits trial rate
- Non-Goal: Peak performance
- Good results currently for dense linear algebra and (some) DG subkernels







?



Outline

- 4 Playtime!
 - Fun with Reduction





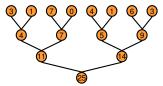
- 4 Playtime!
 - Fun with Reduction





Parallel Reduction

Tree-based approach used within each thread block



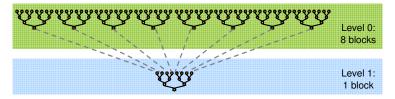
- Need to be able to use multiple thread blocks
 - To process very large arrays
 - To keep all multiprocessors on the GPU busy
 - Each thread block reduces a portion of the array
- But how do we communicate partial results between thread blocks?

Slides by M. Harris (Nvidia Corp.)



Solution: Kernel Decomposition

Avoid global sync by decomposing computation into multiple kernel invocations

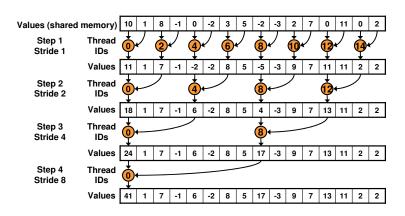


- In the case of reductions, code for all levels is the same
 - Recursive kernel invocation

Slides by M. Harris (Nvidia Corp.)



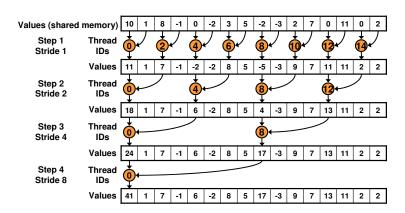
Interleaved Addressing



Slides by M. Harris (Nvidia Corp.)



Interleaved Addressing

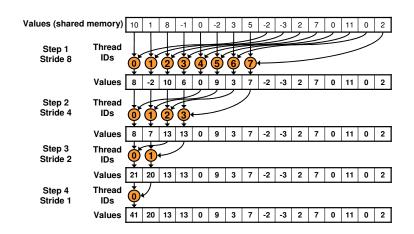


Issue: Divergence

Slides by M. Harris (Nvidia Corp.)



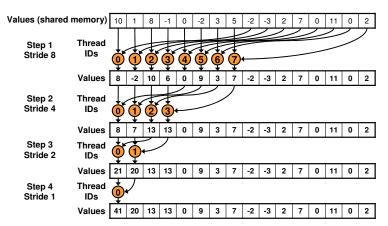
Sequential Addressing



Slides by M. Harris (Nvidia Corp.)



Sequential Addressing



Better!

Slides by M. Harris (Nvidia Corp.)



Reduction: Further Strategies

Further Strategies:

- Exploit SIMD synchronicity
 - Eliminate a few barrier()s
- Amortize cost of index calculation/preparation
 - Not just one item per thread!
- Do as much as possible at compile time
 - Unroll loops
 - Exploit compile-time knowledge of block size, etc.
 - $(\rightarrow \mathsf{metaprogramming} \colon \mathsf{PyCUDA} \; \mathsf{or} \; \mathsf{C} \mathsf{++} \; \mathsf{templates})$





Try for yourself: Performance of GPU Reduction

- In your home directory, find and run 3-reduction/reduction.py.
- 2 Add event-based timing. Compute memory throughput in GiB/s for a number of vector sizes. (e.g. 2^k for $k \in \{12, \ldots, 25\}$)
- 3 Implement and benchmark the improvements discussed previously.
- What else is missing for peak performance? (Google?)

PyOpenCL docs: http://documen.tician.de/pyopencl

These slides: http://tiker.net/tmp/scipy10-pyopencl.pdf





Outline

- 1 Intro: GPUs, OpenCL
- 2 GPU Programming with PyOpenCl
- 3 Additional Topics
- 4 Playtime!
- 5 Conclusions
 - A Brief Look at PyCUDA
 - Summary





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$OpenCL \leftrightarrow CUDA: A dictionary$

| OpenCL | CUDA |
|---|-----------------------------------|
| Grid | Grid |
| Work Group | Block |
| Work Item | Thread |
| kernel | global |
| global | device |
| local | _shared_ |
| ${\tt image} {\it n} {\tt d}_{\tt -} {\sf t}$ | texture <type, n,=""></type,> |
| <pre>barrier(LMF)</pre> | $_{-}$ syncthreads() |
| get_local_id(012) | threadIdx.xyz |
| get_group_id(012) | blockIdx.xyz |
| get_global_id(012) | – (reimplement) |

BROWN

$\mathsf{PyOpenCL} \xrightarrow{\longleftrightarrow} \mathsf{PyCUDA} \colon \mathsf{A} \ (\mathsf{rough}) \ \mathsf{dictionary}$

| PyOpenCL | PyCUDA |
|----------------------------|--------------------------------------|
| Context | Context |
| ${\tt CommandQueue}$ | Stream |
| Buffer | ${	t mem_alloc / DeviceAllocation}$ |
| Program | SourceModule |
| Kernel | Function |
| Event (eg. enqueue_marker) | Event |



Whetting your appetite

```
import pycuda.driver as cuda
import pycuda.autoinit
import numpy

a = numpy.random.randn(4,4).astype(numpy.float32)
a_gpu = cuda.mem_alloc(a.nbytes)
cuda.memcpy_htod(a_gpu, a)
```

[This is examples/demo.py in the PyCUDA distribution.]



Whetting your appetite

3

5

6

8 9

10 11 12

13

14

15

```
mod = cuda.SourceModule("
    __global__ void twice(float *a)
      int idx = threadIdx.x + threadIdx.y*4;
      a[idx] *= 2;
func = mod.get_function("twice")
func(a_gpu, block=(4,4,1))
a_doubled = numpy.empty_like(a)
cuda.memcpy_dtoh(a_doubled, a_gpu)
print a_doubled
print a
```

Whetting your appetite

3

5

6

8 9

10 11

12 13

14 15

```
mod = cuda.SourceModule("
    __global__ void twice(float *a)
      int idx = threadIdx.x + threadIdx.y*4;
      a[idx] *= 2;
                                                 Compute kernel
func = mod.get_function("twice")
func(a_gpu, block=(4,4,1))
a_doubled = numpy.empty_like(a)
cuda.memcpy_dtoh(a_doubled, a_gpu)
print a_doubled
print a
```

Whetting your appetite, Part II

Did somebody say "Abstraction is good"?



Whetting your appetite, Part II

```
import numpy
import pycuda.autoinit
import pycuda.gpuarray as gpuarray

a_gpu = gpuarray.to_gpu(
    numpy.random.randn(4,4).astype(numpy.float32))

a_doubled = (2*a_gpu).get()
print a_doubled
print a_gpu
```



Outline

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Concluding Remarks

- GPU Computing is maturing.
 Now is a great time to start looking at GPUs.
- First factor of 5-10 is usually easy to reach.
- Second factor of 5-10 is a bit harder
 - Usually involves rethinking the algorithm
- Fun time to be in computational science
- Python makes GPUs even more fun
 - With no compromise in performance
- OpenCL presents a huge opportunity:
 - A JIT compiler in a library
 - CPU backends exist (AMD, Apple)
 - → Like weave/codepy/Cython's pyximport, but un-hacky





Questions?

?

Thank you for your attention!

http://mathema.tician.de/software/pyopencl

▶ image credits



Image Credits

■ Isaiah die shot: VIA Technologies

■ RV770 die shot: AMD Corp.

Nvidia Tesla Architecture: Nvidia Corp.

C870 GPU: Nvidia Corp.Context: sxc.hu/svilen001

■ Queue: sxc.hu/cobrasoft

■ RAM stick: sxc.hu/gobran11

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■ Nvidia Tesla Architecture: Nvidia Corp.

■ RV870 Architecture: AMD Corp.

■ Dictionary: sxc.hu/topfer

