Introduction into Hardware and parallel concepts

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Gundolf Haase: Tutorial I

25 years in computing - What has changed?



Gundolf Haase: Tutorial I





- ▶ 1986: 3rd year teacher student + prof
 - Visualization of mesh functions
 - Cubic Splines
 - KC 85/3, 64kB
 - Basic, Pascal, Assembler

teacher Ma/Ph \longrightarrow mathematician

Transputer \longrightarrow BBC-report in 1986



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1989: T805

Transputer T805 [INMOS]: 30 MHz, 4.6 MFLOPS, 8 MB (400 MB/s); Occam $10 \times$ faster than IBM-PC; approx. 3000 EUR





- M. Pester [TU Chemnitz] visited Bulgaria [IICT]
- ▶ U. Langer + A. Meyer + G.H.: DD methods; ASM and MSM,

hierarchical preconditioners, multigrid

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2014: Nvidia Tesla K40: 745 MHz, 1.3 TFLOPS(d), 12GB (250 GB/s); CUDA $10 \times$ faster than a CPU; approx. 3000 EUR

Multigrid for PDEs 1988-90

- Multigrid preconditioners [Jung, Langer, et al.]
- Multigrid software package [Globisch, Langer]
- Multigrid methods for interface problems [Jung, Langer]
- Full-Multigrid-Newton in electromagnetics [Heise]
- MG in mechanical and thermo-mechanical problems [Steidten]
- Domain decomposition methods with numerical tests on the 4-transputer board [Haase, Langer, Meyer].





Computer speed

	multigrid levels unknowns	9 grids 261, 121	14 grids 268 · 10 ⁶	$\begin{array}{c} 15 \hspace{0.1 cm} { m grids} \\ 1 \cdot 10^9 \end{array}$
processor	year	7.4 MB	14 GB	51 GB
T805 (30 MHz), 8 MB, Parix 1.0 T805 (30 MHz), 8 MB, Parix 1.2 i486DX (33 MHz), 8 MB, Linux Xplorer-M601 (32 MB), 32 MB, Parix 1.2 Pentium (133 MHz), 16 MB, DOS 6.2 Pentium-II (350 MHz), 128 MB, Linux Dual Xeon (2.4GHz), 4 GB, Linux Core i7-2600K (3.4 GHz), 16 GB, Ubuntu 10.04	1990 1993 1993 1995 1996 1999 2002 2011	143.00 98.00 41.00 4.60 12.80 1.25 0.23 0.05	49	
Xeon X5660 (2.8 GHz), 96 GB, Ubuntu 11.04	2011	0.05	58	234

Table : Time in seconds for solving the Poisson equation on one proc/core

single core: 3000 times faster (1.5 per year) another factor of 10-35 in case of one GPU $10^3 - 10^7$ CPU-cores available

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2014: Heart simulation [CARP: Plank/Vigmond]

- bidomain equations, large non-linear deformation, CFD (video)
- > Finite element mesh with tetrahedral and hexahedral elements
- Mesh decomposition by METIS





Solve linear system of equations (That is our part!)

$$Ku = f$$

in each outer (time/non-linear) iteration.

- System matrix *K* is sparse but unstructured.
- 27 Mill. d.o.f. in 1 sec. on 256 cores.

Oxford Benchmark - bidomain equations

40.992.163 Elements; 6.901.583 d.o.f; real time duration: 250 ms





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toolbox (CPU \blacksquare /GPU \Box) vs. Petsc (hypre) \propto on mephisto and hector [II/2012]



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Heterogeneous many-core processors

- GPU: 250 GByte/sec. memory bandwidth 1310 GFLOPS (double prec.)
- 16 × 32 cores; SIMD + MIMD on (partially) non-coherent shared memories + CPU
- Programming in CUDA (OpenCL) + MPI
- ► GPU 10-100 times faster than one CPU-core.
- \blacktriangleright 10 \times better price/performance ratio [consumer GPU]
- GPU self-assembled 4–GPU server [2008] self-assembled fermi server [2010]
- mephisto: GPU cluster in Graz [Aug. 2011]
 5× (4× Tesla 2070 + 12 cores; 24 + 96 GB)
 (4× Tesla K20X + 16 core),
 (1× Xeon Phi + 16 core) [Aug. 2013]
 17 Tflops peak performance (DP);
 Infiniband QDR (40Gb/s)

Extension of mephisto by $2 \times (4 \times$ Xeon Phi + 16 cores; 32 + 256 GB) [2015]







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Green IT

David Shaw [BBC-report in 1986, see link]:

"There is one critical problem with that [supercomputers] and that is heat.

... The latest supercomputers [Cray X-MP/48] really are very small, very highly efficient refrigerators."

- Cray-2 in 1986: peak 1.9 Gflops, 200 kW, 0.0095 Mflops/Watt
- Tianhe-2 in 2014: 1902 MFLOPS/Watt
- Titan in 2014: 2142 MFLOPS/Watt
- Sequoia in 2014: 2177 MFLOPS/Watt
- Mflops per Watt improved 200 000 times!

(12C Xeons + Xeon Phi 31) (16C Opteron + Tesla K20) (Blue Gene/Q, Power 16C)

- 김씨 제 문 제 제 문 제

What do you have to expect?



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Tutorial with practical work

- Parallel concepts; Hardware; Relations inbetween; The example environment
- II) PDE; Finite Element discretization; System of equations; (simple) iterative solver; parallelization concept
- III) Classical shared memory and distributed parallelization parallelization (OpenMP and MPI)
- IV) Accelerator programming for NVIDIA GPU; practical work (OpenACC and CUDA)
- V) Distributed computing with multiple GPUs; practical work

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Parallel concepts



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Classification by memory access

- Distributed memory access
 - cluster computing; multi-core computing
 - MPI (Message Passing Interface)
- Shared memory access
 - multi-core computing, many-core computing
 - OpenXXX, CUDA, OpenCL
 - distributed shared memory on compute clusters available.
- Faked shared memory access
 - distributed shared memory on compute clusters available (hardware!!).
 - PGAS (partitioned global address space)

UMA: uniform memory access

NUMA: non-uniform memory access

ccNUMA: cache coherent NUMA

hUMA: heterogeneous UMA (by AMD)

bandwidth: byte per second in a data transfer from/to memory $(O(\frac{1}{t_{bandwidth}}))$ **latency**: time until data transfer starts $t_{latency}$ Transferring *n* Byte: $t(n) = t_{latency} + n * t_{bandwidth}$

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Memory hierarchies

- Normal DRAM (Dynamic Random Access Memory) stores a bit in a capacitor
 - needs only a few transistors \implies small area on chip, cheap
 - large amount of memory
 - needs refreshment cycles slow access
- Cache SRAM (Static Random Access Memory) stores a bit in a flip-flop circuit
 - needs more transistors => larger area on chip, expensive
 - small amount of memory
 - ▶ no refreshment cycles ⇒ fast access
- Therefore, DRAM is combined with a hierarchy of smaller but faster caches.

Non Uniform Memory Access (wrt. latency and bandwidth)

```
    CPU:
Register - L1 - L2 - L3-cache - memory - remote memory
```

► GPU:

Register – shared/L1 – L2 – GPU memory – CPU memory

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Classification by streams [Flynn, 1966]

Data stream vs. Instruction stream

Instruct	ion Stream		
Single	Multiple		
SISD	MISD	Single	Data

Table : Flynn's taxonomy

SISD (Single Instruction Single Data) is the classical sequential von-Neumann computer.

MISD (Multiple Instruction Single Data) can be found in the pipelining of instruction in modern processors and in flight control computers.

Our focus will be on MIMD and SIMD.

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MIMD - Multiple Instructions Multiple Data

- Each process (and its instructions) access data on different ressources (i.e., distributed memory)
- Often as SPMD (Single Programm Multiple Data)
- explicit access to ressources of other processes via communication.
- $\blacktriangleright \implies dead \ locks \ might \ block \ the \ whole \ code$
- MPI (Message Passing Interface)

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Dead lock: Dinner for five [Dijkstras 1971]

Dead lock: Processes have to wait for an event that has to be performed by one of the waiting processs.



5 philosophers (P) with 5 forks (R). Each P needs two forks (R) for eating:

- Each philospher takes the the right fork and waits for the left fork. ⇒ Dead lock for all (starving with one fork in their hand)
- 2. Wait until both forks are available, eat and release them afterwards \implies Dead lock for one (P_1, P_3) eat alternating with (P_5, P_2) and P_4 starves

A dead lock for all is obvious but a dead lock for one might be very subtle to find.

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SIMD - Single Instruction Multiple Data

- Each thread (and its instructions) accesses data on shared ressources (e.g., shared memory)
- implicit access to ressources of other threads.
- $\blacktriangleright \implies$ data races result in unpredictable (incorrect) results
- OpenXXX, CUDA, OpenCL
- A SIMT (Single Instruction Multiple Threads) per warp on GPUs available.
 - 1 instruction pointer per b threads in one warp
 - all b threads have to wait for slowest thread (alternatives, while-loops)

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Data Race

Uncoordinated manipulation of shared ressources.

thread A: $N := N + 1$	clock.	thread B: $N := N - 1$
load N	(1)	load N
inc N	(2)	dec N
store N	(3)	store N

The value of N is not predictable, it depends on the execution speed of threads A and B



Data race: solution

- Consider the operations load, inc/dec, store as one atomic operation.
- This atomic operation has to be finished before another thread gets access to the ressources.
- $\blacktriangleright \implies N$ will be locked.
- N in local cache requires ccNUMA (Hey, that value has been changed!).
- For-loops for vector operation <u>z</u> = α · <u>z</u> + <u>y</u> followed by <u>a</u> = <u>z</u> + <u>b</u> might require thread synchronization between loops.
 (#pragma omp barrier)

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What is new in accelerator programming?



- 2 levels of shared memory on GPU: global for GPU + local on SM
- Host: Usually a CPU core
- Device: Accelerator device as GPU or Xeon Phi (or multi-core CPU)
- seperate memory with explicit data transfer between host and device memory
- memory(host) >> memory(device)
- bandwidth(host) < bandwidth(device)</p>
- Synchronization between threads only locally on SM, not globally.
- Threads in one warp are parallel by instruction (one IP for all)

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Hardware remarks



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Processor types on the market



18 cores, 1.5TB 108 GByte/sec ≈750 GFLOPS(d,peak) AVX2 (512) 145 Watt SIMT/SIMD (MIMD) g++, OpenMP

Cluster on DIE;





 $\begin{array}{l} 15\times192 \text{ cores, } 12 \text{ GB} \\ \hline 288 \text{ GByte/sec} \\ 1.4 \text{ TFLOPS (d,peak)} \\ 235 \text{ Watt} \end{array}$

SIMT + MIMD CUDA, OpenACC

incl. GPUs + OpenACC;

MIC Xeon Phi 7120P



61 cores, 16 GB 352 GByte/sec 1.2 TFLOPS (d,peak) AVX (512) 300 Watt SIMT/SIMD (MIMD) Intel-Compiler, OpenMP 4.0

MIC (Many Integrated Core);

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Programming Models in multi-/many-core environments

distributed memory: MPI

vectorization: SSE, AVX → compiler support (#pragma omp simd)
 shared memory: OpenMP → compiler support (#pragma omp parallel for)
 many-core:

 GPU-systems: CUDA, OpenCL, OpenACC (→ general devices)
 general: OpenACC (#pragma acc parallel loop) commercial compiler support since spring 2012 [Nov 13, 2011; Cray, Nvidia, PGI]
 MIC-systems: OpenMP 4.0 (→ general devices) (#pragma omp target) [July 2013: AMD, Cray, Intel, IBM, NVIDIA, ...]

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Shared memory: first example



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seq: Scalar product

$$s = \langle x, y \rangle = \sum_{k=0}^{N-1} x_k \cdot y_k$$

Listing 1: Scalar product

```
double scalar(int N, const double x[], const double y[])
{
    double sum = 0.0;
    for (int i=0; i<N; ++i)
    {
        sum += x[i]*y[i];
    }
    return sum;
}</pre>
```

dualhex: $2 \times$ AMD Opteron 2427, 6x 2.20GHz, 32 GB N=250 Mill., 50 outer loops

1 core: 0.78 sec.

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shm: Scalar product - race condition

Listing 2: Scalar product with race condition

```
double scalar(int N, const double x[], const double y[])
{
    double sum = 0.0;
    #pragma omp parallel for private(i) shared(x,y,sum)
    for (int i=0; i<N; ++i)
    {
        sum += x[i]*y[i];
    }
    return sum;
}</pre>
```

dualhex: N=250 Mill., 50 outer loops

4 cores: 0.81 sec.

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Easy, but wrong result because of data race.

shm: data race - two cooks

Listing 3: Scalar product with data race

```
double scalar(int N, const double x[], const double y[])
{
    double sum = 0.0;
#pragma omp parallel for private(i) shared(x,y,sum)
    for (int i=0; i<N; ++i)
    {
        sum += x[i]*y[i];
     }
     return sum;
}</pre>
```





shm: Scalar product - atomic

Listing 4: Scalar product with atomic pragma

```
double scalar(int N, const double x[], const double y[])
{
    double sum = 0.0;
#pragma omp parallel for private(i) shared(x,y,sum)
    for (int i=0; i<N; ++i)
    {
    #pragma omp atomic
        sum += x[i]*y[i];
    }
    return sum;
}</pre>
```

dualhex: N=250 Mill., 50 outer loops

4 cores: 38 sec.

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correct result but slow because of atomic operation.

shm: Scalar product - reduce

Listing 5: Scalar product with reduction

dualhex: N=250 Mill., 50 outer loops

4 cores: **0.48 sec.** (1 core: 0.78 sec.)

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Easy, correct result.

Shared Memory: speedup



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Shared memory: non-Newtonian fluid

Diego A. Vasco [Universidad de Santiago de Chile]

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Solve linear system in each inner step

- ▶ system of coupled non-linear second order PDEs $\stackrel{\rm SIMPLE}{\Longrightarrow}$ sequence of linear PDEs.
- unit cube, 7-point difference stencil



- Gauss-Seidel (forw/backw) wrt. plains in z-direction and
- ADI (Alternating Directions Iterative methods) in each plain
- shm parallel: combine plaines to a block Jacobi with above Gauss-Seidel in each block.



shm: system solve - naive approach

Listing 6: block-Jacobi Gauss-Seidel (shuffling)

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```
!Somp parallel do shared(app) schedule(static)
do k = 1, N // plain k: forward
.....
app(i,j,k) = .... // cube data
end do //
!Somp parallel do shared(app) schedule(static)
do k = N, 1, -1 // plain k: backward
....
app(i,j,k) += .... // cube data
end do
....
```

slower than on one thread

shm: system solve - naive approach

Listing 7: block-Jacobi Gauss-Seidel (shuffling)



slower than on one thread

data blocks are remapped onto threads (data transfer!!)

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shm: system solve - better approach

Listing 8: block-Jacobi Gauss-Seidel (no shuffling)

```
Somp parallel shared(app) schedule(static)
tid = omp_get_thread_num() // my thread ID
Isize = int((kend-kst+1)/nthrds)+1 // junk size
kf = tid*lsize + kst // index range for this thread
kl = min(((tid+1)*lsize + kst - 1),kend)
kp = 1 // first forward direction
do nswz = 1,2
do k = kf, kl, kp // plain k
.....
app(i,j,k) = .... // cube data
end do
kp = -kp // reverse direction
end do
```

IMSC-KFU Graz

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shm: system solve - speedup

#threads	PROGRAM	SOLVE	MECFLU	SIMPLE	CALPH
1	298	85	186	30	51
2	188	54	116	20	32
4	101	28	63	12	17
6	73	18	45	9.2	10
8	61	15	37	8.6	66
12	47	10	27	8.6	7.5
speedup	6.3	8.4	6.8	3.6	6.7

Speedup on dualhex, time in min.

- good speedup of 8.4 in SOLVE
- poor speedup of 3.6 in SIMPLE
 unnecessary reduce directive for an array (OpenMP 3.0)
 extra parallel–loop for boundary data ⇒ data shuffling
- speedup of 6.7 in update (vectors and material coeff.) can be further improved by avoiding above data shuffling

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Listing 9: Handling of boundary data (shuffling)



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Listing 10: Handling of boundary data (no shuffling)



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shm: system solve - Aug. 2011

#threads	PROGRAM	SOLVE	MECFLU	SIMPLE	CALPH
speedup July'11	6.3	8.4	6.8	3.6	6.7
speedup Aug'11	11.7	11.4	11.8	11.3	11.1

dualhex: Speedup with 12 threads

- no reduce arrays (SIMPLE)
- sequential handling of boundary data (no data shuffling)
- temp. data are always private (MECFLU)!
- no dynamic memory allocation in threads
- larger scope for #pragma omp parallel (PRAGMA)
- beware of data race in loop dependencies (\downarrow) for pre-computed data

Nov. 2013: 4-year project in Chile for D. Vasco

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shm: pitfall for polynom: $p = \sum_{k=0}^{N} a_k \cdot x^k$

Listing 11: Polynom sequentially

```
\begin{array}{l} p &= 0.0 \\ xk &= 1.0 \\ do \ k &= 1, \ N+1 \\ p &= p + a(k) * xk & ! \ add & a_{-k} * x^{-}k \\ xk &= xk * x \\ end \ do \end{array}
```

Listing 12: Polynom shm (wrong result)

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shm: correct for polynom

$$\rho = \sum_{k=0}^{N} a_k \cdot x^k = \sum_{\text{tid}=0}^{\text{nthrds-1}} \sum_{k=kf_{\text{tid}}}^{kf_{\text{tid}}} a_k \cdot x^k$$

Calculate for thread tid its index range [kf,kl] explicitely.

Listing 13: Polynom shm

```
p = 0.0
!$omp parallel private(k,xk) shared(a) reduction(+:p)
 tid = omp_get_thread_num() ! my thread number
 |size = int((N+1)/nthrds)+1 | my max. portion of data
 kf = tid * lsize+1
                                 ! interval
    = min(kf+lsize, N+1)
 kΙ
                                 I correct x^k for this thread
 xk = x * * (kf - 1)
 do k = k\hat{f}, kl
    p = p + a(k) * xk
    xk = xk * x
 end do
!$omp parallel
                                 ! correct result
```

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Examples: programming environment



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Getting the code

- Download code (link)
- unzip: > tar xzf Chile.tgz
- change into an environment shm: > cd shm
- change into a subdirectory: > cd skalar
- compile, link and run: > make run

Each directory contains at least *skalar* and jacobi, partially also with its MPI paralleliazion therein.

- > cd shm; ls *default.mk lists all supported compilers (here: GCC_, ICC_, PGI_)
- > cd skalar; make COMPILER=ICC_ run uses the Intel-compiler.

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Supported parallel environments

- Sequential in directory seq.
- OpenMP 3.0 in directory shm.
- ▶ MPI in directory par.
- CUDA in directory CUDA.
- OpenACC in directory OpenACC.
- MIC (MIC-pragmas / OpenMP 4.0) in directory MIC.
- MPI+OpenMP in directory OpenACC/par*.
- MPI+CUDA in CUDA/par*.
- MPI+OpenACC in OpenACC/par*:

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